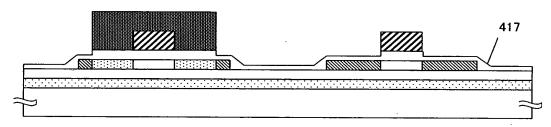


FIG.6B



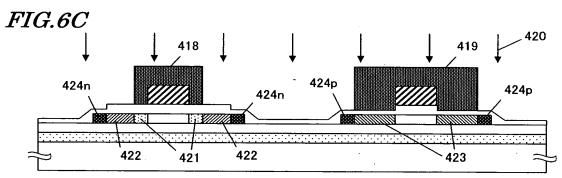
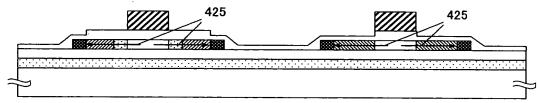
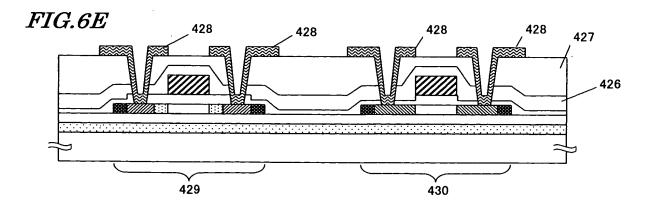


FIG.6D





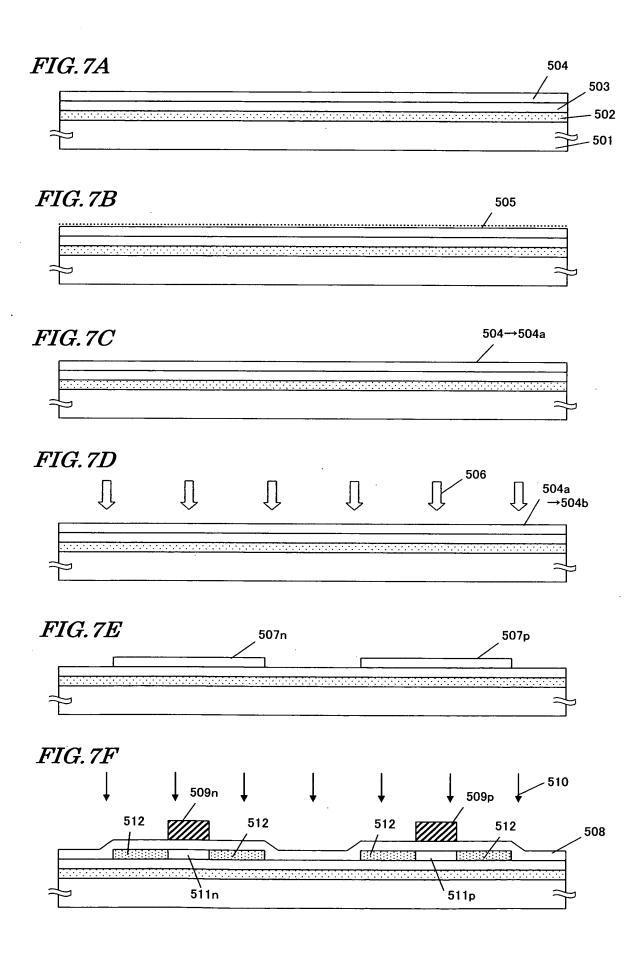
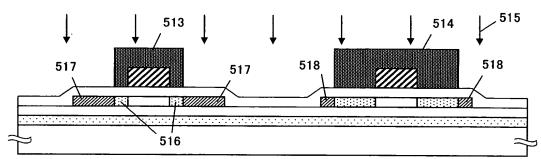
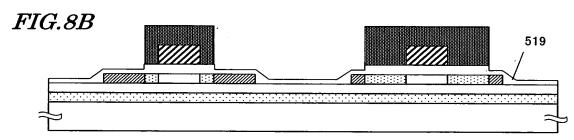


FIG.8A





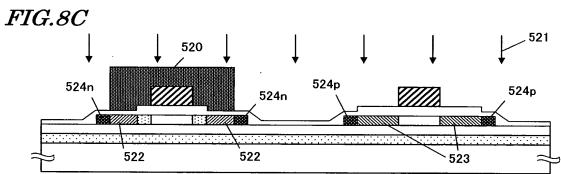
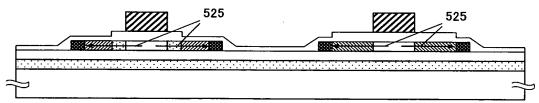
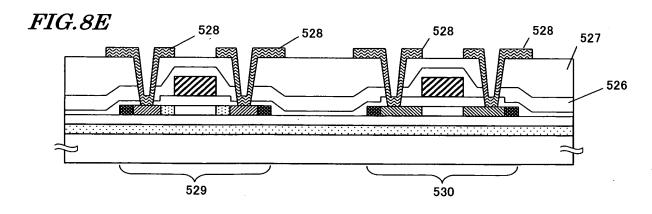
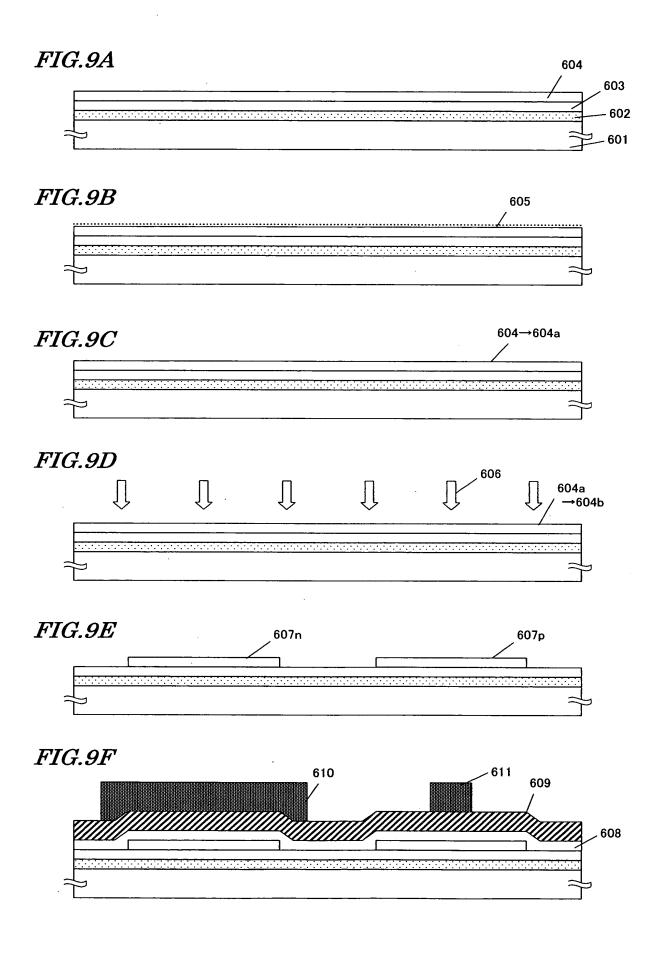
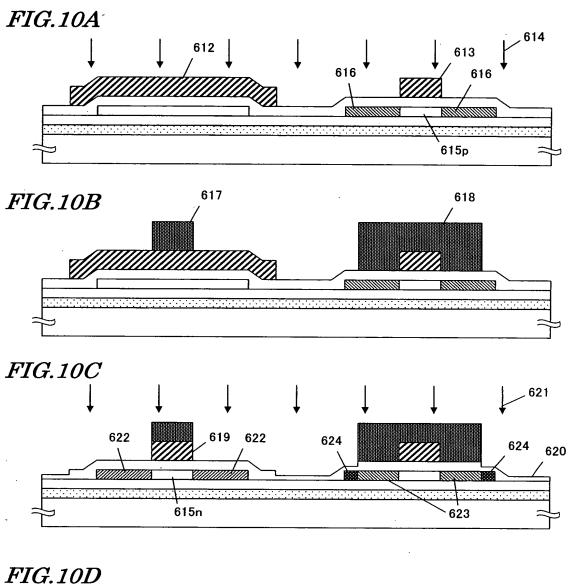


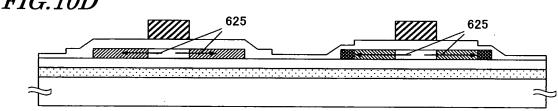
FIG.8D

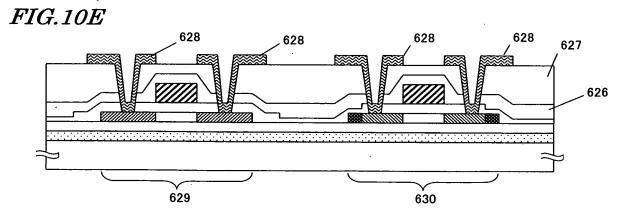












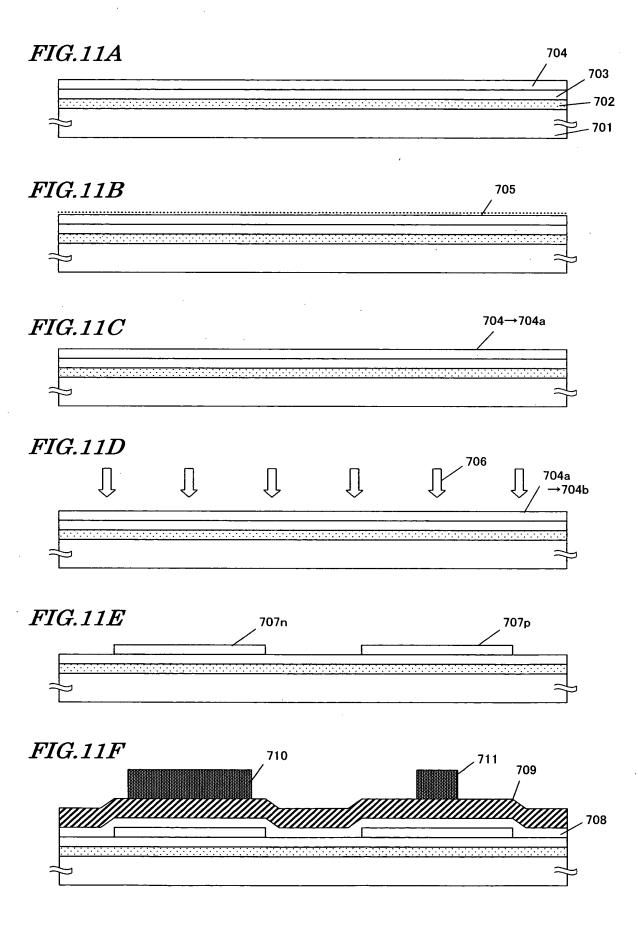
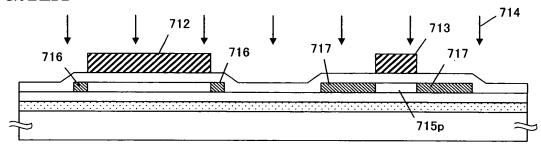
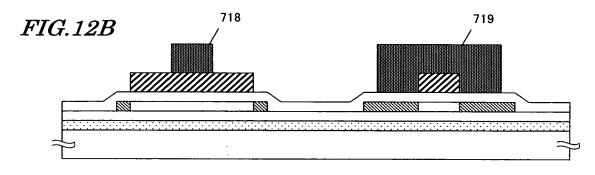


FIG.12A





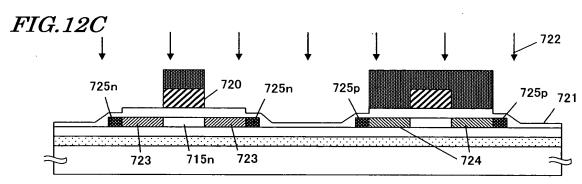
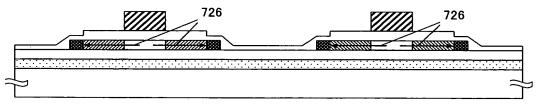
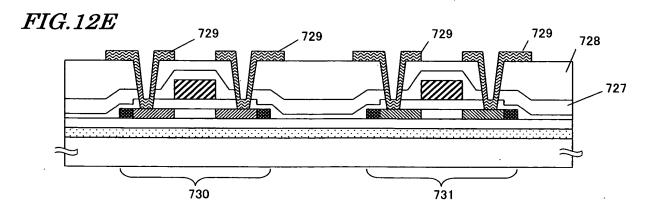
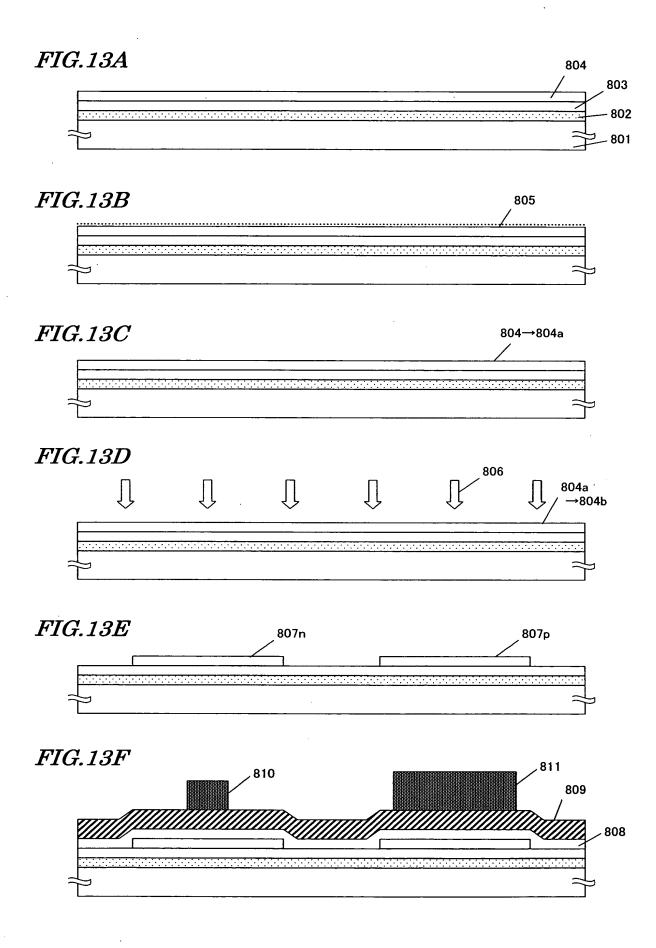
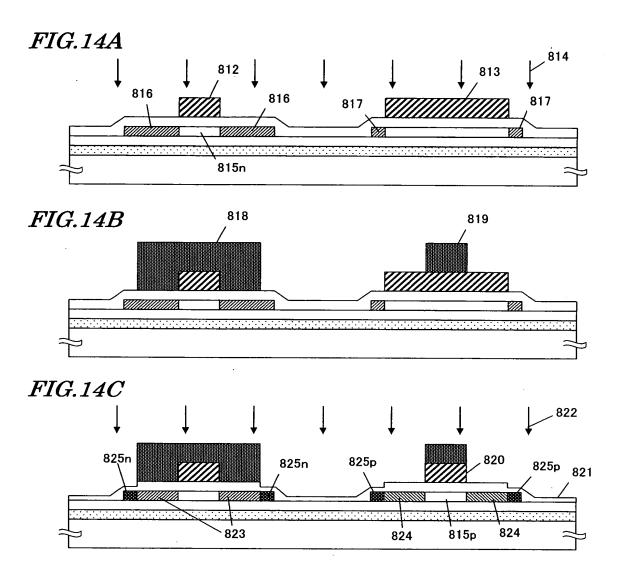


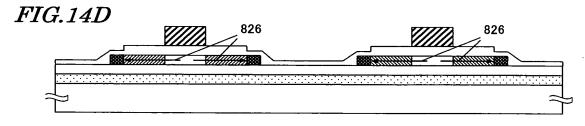
FIG.12D











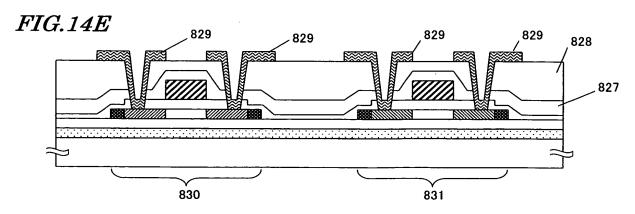
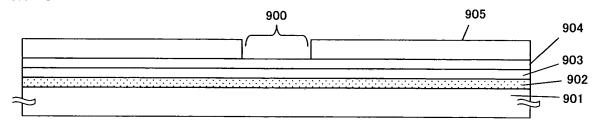
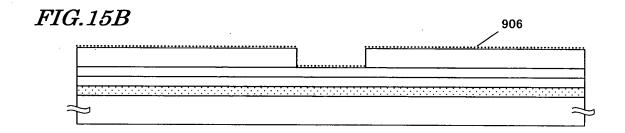
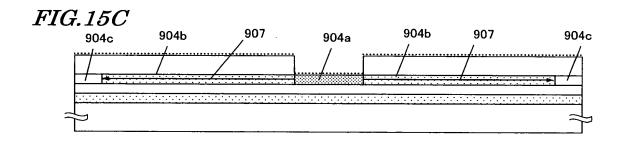
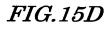


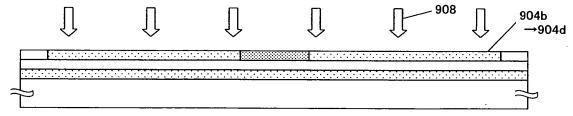
FIG.15A

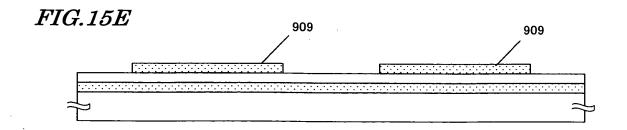












15a *FIG.16A* 11a 12a 14a 16a 13a 15b *FIG.16B* 11b 12b 14b \ 16b 13b 17b 15c *FIG.16C* 13c 11c 12c 14c \| 16c 17c *FIG.16D* 15d 11d ,12d

FIG. 16D

13d

11d

12d

14d

16d

17d

FIG. 17A 15e 11e 12e 11e 14e 16e 19e 17e

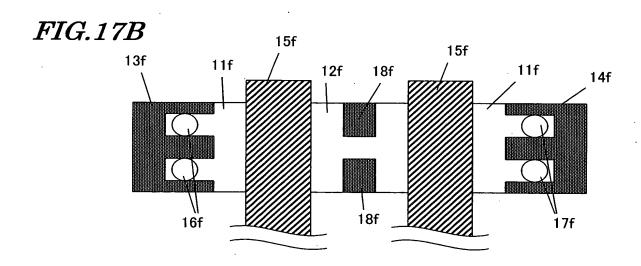
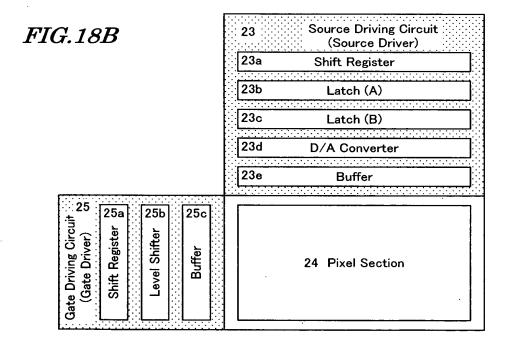


FIG.18A Source Driving Circuit 20 (Source Driver) 20a Shift Register 20b Buffer 20c Sampling Circuit Gate Driving Circuit & (Gate Driver) 22a 22b 22c Shift Register Level Shifter Buffer 21 Pixel Section



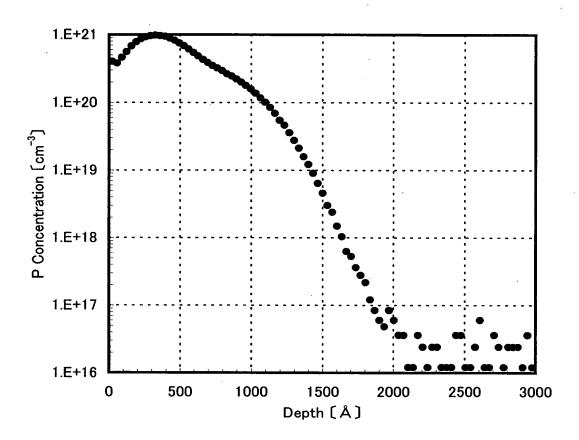


FIG.20A

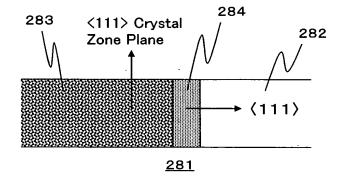


FIG.20B

